Mini-Project 3

UBC Elec 301

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Part 1 Part 1 The Cascode Amplifier:

First, we are tasked with simulating and recording the behavior of a cascode amplifier built out of 2 2N3904 npn transistors. The minimum specifications of our amplifier are as follows:

R_{out} (value at mid band)	R_{in} (minimum value at mid band)	$\|A_v\|$ (minimum value at mid band)	f_L (maximum value)
2.5 kΩ ± 250Ω	5 kΩ	50	500 Hz

Resistors

In order to bias our cascode, we employ the 1/4th rule for determining our resistor values.

The 1/4th rule states that:

V_{C2} = ¾ Vcc, $V_{E2} = V_{C1}$= ½ Vcc, V_{E1} = ¼ Vcc and I_1= 0.1*I_{E2}.

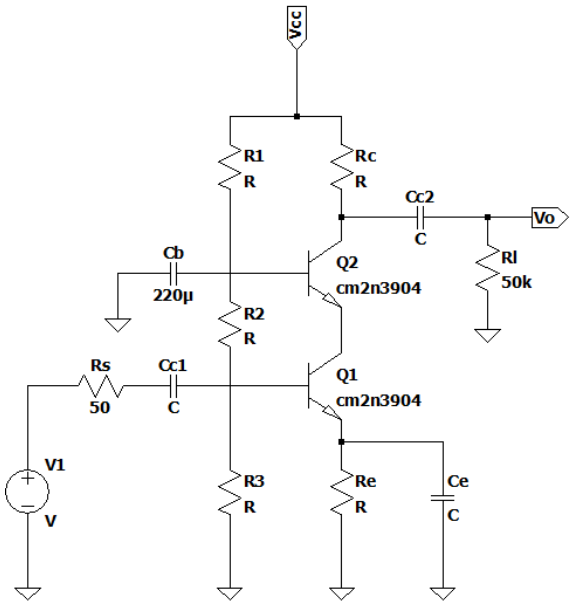

Figure 1-1: initial circuit information

Carrying over from the previous mini project we found the β value of our 2N3904 transistors to be about 118 and as usual we assume a V_{be} of 0.7V

Using the fact that we want a maximum R_{out} of around 2.5k at midband we can say that our resistor R_C = 2.5k since at midband the output of our amplifier is isolated from the rest resulting in an output resistance entirely dependent on R_C setting R_C = 2.5k we can calculate the rest of our values like this:

$$Vcc = 20V, V_{C2} = 15V, V_{E2} = V_{C1} = 10V, V_{E1} = 5V, V_{B2} = 10.7V, V_{B1} = 5.7V,$$

$$I_{C2} = \frac{5}{R_C} = 2mA = \beta * I_{B2} \therefore \boldsymbol{I_{B2}} = 16.94\mu A\,, \qquad I_{C2} + I_{B2} = I_{E2} = \boldsymbol{I_{C1}} = 2.017mA$$

$$\boldsymbol{I_{B1}} = \frac{I_{C1}}{\beta} = 17.092\mu A\,, \qquad I_{E1} = I_{C1} + I_{B1} = 2.034mA \ \therefore \ \boldsymbol{I_1} = 0.2034mA$$

$$I_1 - I_{B2} = \boldsymbol{I_2} = 186.455\mu A, \boldsymbol{R_E} = 2458$$

$$\boldsymbol{R_1} = \frac{20 - 10.7}{I_1} = 45721, \qquad \boldsymbol{R_2} = \frac{10.7 - 5.7}{I_2} = 26816, \qquad \boldsymbol{R_3} = \frac{5.7}{I_2 - I_{B1}} = 33655$$

Using our list of standard resistor values the resistors are as follows:

R_1 =47k, R_2 =27k, R_3 =33k, R_C =2.7k, R_E =2.4k

These bias resistors result in the following DC operating point of our cascode amplifier.

V(vcc)V:	V(vb2)V:	V(vb1)V:	V(vc)V:	V(vm)V:	V(ve)V:
20	10.5833	5.5907	14.5429	9.91778	4.92503
Ic(Q2)A:	Ib(Q2)A:	Ie(Q2)A:	Ic(Q1)A:	Ib(Q1)A:	Ie(Q1)A:
0.00202116	1.54421e-5	0.0020366	0.0020366	1.54974e-5	0.0020521

Using this information about the DC operating point we can recalculate β = 130. We also use this information to determine our small signal parameters $gm = \frac{I_c}{V_T} = \frac{0.002036}{0.025} = 0.081 \ and \ \frac{0.00202116}{0.025} = 0.0808$ for Q1 and Q2 respectively and $r_\pi = \frac{\beta}{gm} = 1608 \ and \ 1620$ for Q1 and Q2 respectively. Since Q1 and Q2 are identical transistors from this point on we will assume they have the same small signal parameters and set **β = 130, r_π = 1.6kΩ, gm = 0.08S** for both transistors. However, having found our r_π we can now see that our midband input impedance does not meet specifications. At midband our input impedance should theoretically be equivalent to $R_3 \parallel R_2 \parallel r_\pi$ which initially is found to be about 1.4k. we adjust this by adding a resistor R4 to our input, when we calculate input impedance our equation becomes $(R_3 \parallel R_2 \parallel r_\pi) + R4$ thus meeting our specifications if R4 = 3600

The size of R4 directly affects our midband gain. After adding the resistor R4 the equation for our gain becomes:

$$-gm(R_C \parallel R_L) * \frac{R_2 \parallel R_3 \parallel (r_\pi)}{[R_2 \parallel R_3 \parallel (r_\pi)] + R_S + R4}$$
$$= -0.08 * (2561) * \left(\frac{1444}{5094}\right) = -58.1 \frac{V}{V}$$

Which manages to meet the requirements of $|50| \frac{V}{V}$

Recalculating our dc operating point after adding the small resistor we see that there haven't been any significant changes so we will continue to use the previously calculated values of β, gm and r_π.

Capacitors

As with the previous mini project we will be using the equations below to calculate our C_π and C_μ. For V_{CB} I used the value 4 V because The V_{CB} measure for Q1 and Q2 were 4.32 and 3.95 respectively, so I took an approximate value of 4 in order to use the same C_π and C_μ for both transistors.

$$C\pi = 2 * CJE + TF * gm, \qquad C\mu = \frac{CJC}{\left(1 + \frac{V_{CB}}{VJC}\right)^{MJC}}$$

$$C_\pi = 2 * 4.5p + 400p * 0.08 = 41pF \ , C_\mu = \frac{3.5p}{\left(1 + \frac{4}{0.750}\right)^{0.330}} = 1.9pF$$

We can see from the low frequency small signal model that Cc1 is decoupled from the rest of our circuit and its position will not be affected by the other low frequency poles.

$$\omega_{lp1} = \left(C_{C2} * (R_L + R_C)\right)^{-1} = \ (C_{C2} * 52700)^{-1}$$

$$\omega_{lp2} = (C_{C1} * (R_s + R4 + \left(R_2 \parallel R_3 \parallel (r_\pi + (1+\beta) * R_E)\right))) \ ^{-1} = \ (C_{C1} * 17833)^{-1}$$

$$\omega_{lp3} = \left(C_E * (\left(\frac{((R_s + R4) \parallel R_2 \parallel R_3) + r_\pi}{1+\beta}\right) \parallel R_E)\right)^{-1} = \ (C_E * 34.08)^{-1}$$

As with the previous mini project we have a zero associated with the point where our emitter's admittance goes to 0 $\omega_{lz1} = (C_E * R_E)^{-1} = (C_E * 2400)^{-1}$
Seeing how the pole caused by C_E is 2 orders of magnitudes larger than the other 2 poles, assuming we choose capacitors within the same order of magnitude for the 3 of them we will see that The pole associated with C_E will dominate making it mostly responsible for the position of the low 3db cut point of our amplifier. Seeing as the zero is also associated with C_E it's reasonable to assume it will have some effect on the low 3dB point as well, using these observations we can say:

$$500 * 2\pi \geq \omega_{l3dB} = \sqrt{\left(\frac{1}{34.08 * C_E}\right)^2 - 2 * \left(\frac{1}{2400 * C_E}\right)^2}$$

$$C_E \geq 9.34\mu F$$

In order to satisfy the requirement and obtain a larger mid band I set C_E to $22\mu F$. And in order to maintain our assumption that C_E will be the dominant pole we will need to set the remaining capacitors to be of a similar magnitude, so I set them all to be $10\mu F$ for simpler calculations. Resulting in the following Cascode circuit (Figure 1-2)

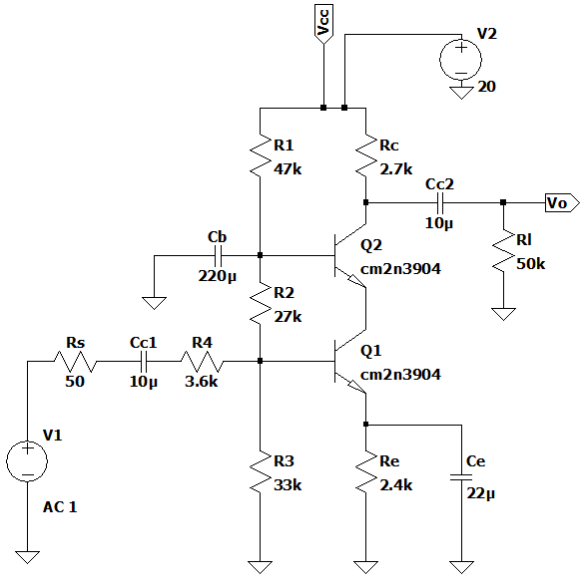

Figure 1-2: My Cascode after all components are chosen

Part A – The dc operating point

Final DC operating point:

V(vcc):V	V(vb2):V	V(vb1):V	V(vc):V	V(vm):V	V(ve):V
20	10.5833	5.5907	14.5429	9.91778	4.92503
Ic(Q2):A	Ib(Q2):A	Ie(Q2):A	Ic(Q1):A	Ib(Q1):A	Ie(Q1):A
0.002021	1.54E-05	-0.00204	0.002037	1.55E-05	-0.00205

Part B – Bode Plot

To find the high Frequency poles we need to model our high frequency circuit and then apply miller's theorem to split it into 2 much more manageable circuits as we have demonstrated in previous mini projects.

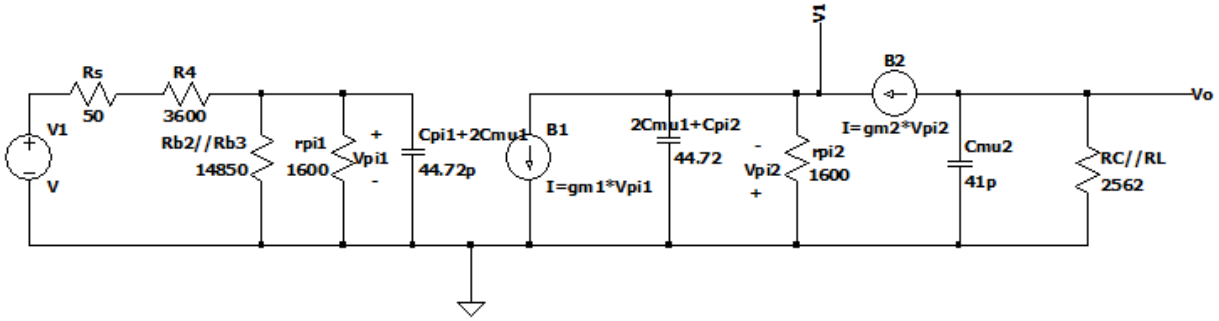

Figure 1-3: the miller equivalent circuit.

Looking at this circuit we can determine our high frequency poles easily. Each of the capacitors are isolated from each other so we can simply use the methods learned in class to form the following equations after accounting for the magnified resistance between emitter and base.

$$\omega_{Hp2} = [((R_S + R4) \parallel R_2 \parallel R_3 \parallel r_\pi) * C_{\pi 1} + 2C_{\mu 1}\ ]^{-1}$$

$$\omega_{Hp3} = \left[\frac{r_{\pi 2}}{1+\beta_2} * (C_{\pi 2} + 2 * C_{\mu 1}\ )\right]^{-1}$$

$$\omega_{Hp1} = \left[(R_C \parallel R_L) * C_{\mu 2}\right]^{-1}$$

Knowing that we set $C_{\mu 2} = C_{\mu 1} = 1.9pF, C_{\pi 2} = C_{\pi 1} = 41pF$ we can find the values of our high frequency poles.

$$\omega_{Hp2} = [(50 + 3600) \parallel 27k \parallel 33k \parallel 1600) * 41p + 2 * 1.9p\ ]^{-1} = 21.6M\frac{rad}{s} = 3.44MHz$$

$$\omega_{Hp3} = \left[\frac{1600}{1+130} * (41p + 2 * 1.9p\ )\right]^{-1} = 1830M\ rad/s = 291MHz$$

$$\omega_{Hp1} = [(2.7k \parallel 50k) * 41p]^{-1} = 9.52Mrad/s\ =\ \ 1.5MHz$$

Seeing that poles 1 and 2 are within a decade of each other its reasonable to say they will both contribute to the high frequency cut point, however the 3rd pole is almost 2 decades larger and will most likely not have much of an effect, therefore we can estimate the high cut frequency as:

$$\frac{1}{\omega_{H3dB}} = \sqrt{\left(\frac{1}{21.6M}\right)^2 + \left(\frac{1}{9.52M}\right)^2} = 8.71M\ rad/s\ =\ 1.39MHz$$

And previously we approximated the low frequency cut point as:

$$\omega_{l3dB} = \sqrt{\left(\frac{1}{34.08 * C_E}\right)^2 - 2 * \left(\frac{1}{2400 * C_E}\right)^2} = 1333.5\,rad/s\ = 212.2Hz$$

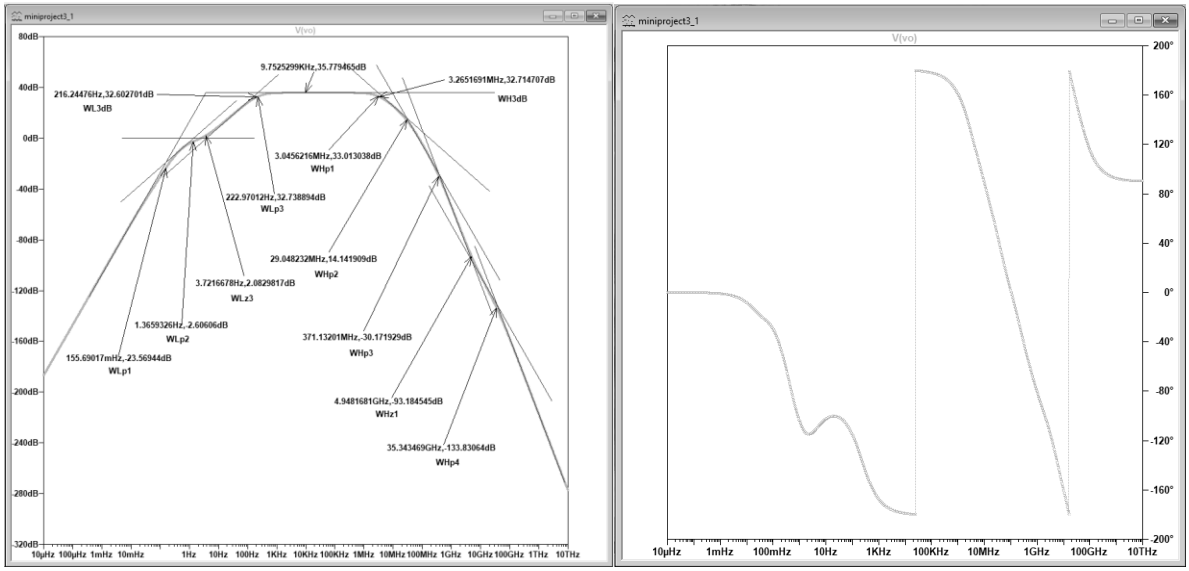

Figure 1-4: Bode Plot of Cascode amplifier Magnitude plot (left), Phase plot(right)

As seen in figure 1-4 the measured 3dB cut frequencies of my amplifier are 222Hz and 3.04MHz for low and high respectively, and the midband gain is measured to be 35.7dB = 60V/V. When compared to my calculated values of 212Hz and 1.39MHz we can see that the low frequency assumption for dominant pole was very accurate and for the high frequency pole our estimate was less so. However, both values fell within a reasonable range of the measured values and by simulating we learned that we have a longer bandwidth than initially assumed which is desirable in an amplifier.

Part C – Saturation point

As can be seen in Figure 1-5 the output voltage tends to reach saturation around the point where the input voltage starts supplying 70mV RMS $\approx 100mV$ peak as was explained in mini project 2, after this point the voltage stops increasing in a linear manner because the transistor supplying the output voltage has reached saturation.

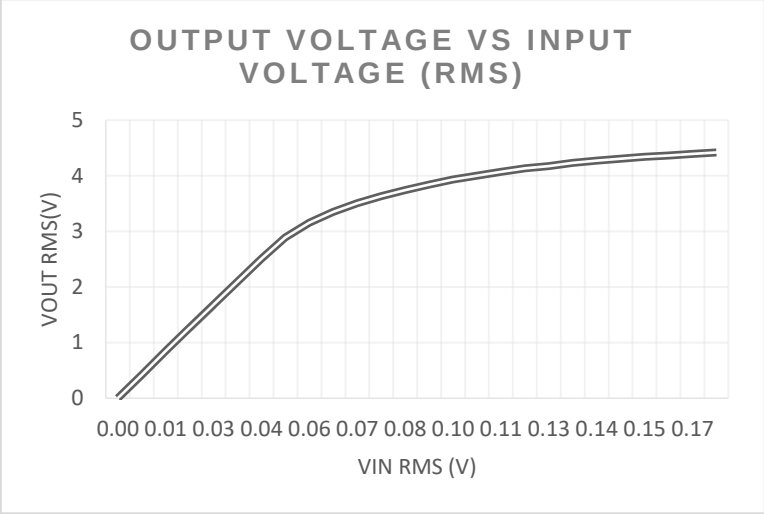

Figure 1-5: Input voltage vs output voltage curve

Part D – Input and output impedance

Our calculated input impedance at midband was $\left(R_3 \parallel R_2 \parallel (r_\pi)\right) + R4 = 5044\Omega$

Applying a 1mV voltage source to our input after removing the source impedance and measuring the current through that source to determine impedance by ohm's law $Z = \frac{V}{I}$ I found the measured input impedance to be 5405Ω meeting our amplifiers input impedance parameter of being greater than 5000Ω

At mid band our output impedance is primarily dependant on R_C and the transistor output resistance r_o, in our case we assume r_o is sufficiently large enough to act as an open circuit meaning our output resistance should be approximately equal to $R_C = 2700\Omega$

Applying a 1mV voltage source to our output after removing the load impedance and measuring the current through that source to determine impedance by ohm's law $Z = \frac{V}{I}$ I found the measured output impedance to be 2710Ω meeting our amplifiers output impedance parameter of being $2500\Omega \pm 250\Omega$

Part 2 Cascaded Amplifiers:

We are initially given the circuit shown in figure 2.1 and asked to design one that meets the following specifications:

At midband it should have an input and output impedance of $50\Omega \pm 5\Omega$, the low frequency cut point should be before 100Hz, and be built using 2n3904 npn transistors.

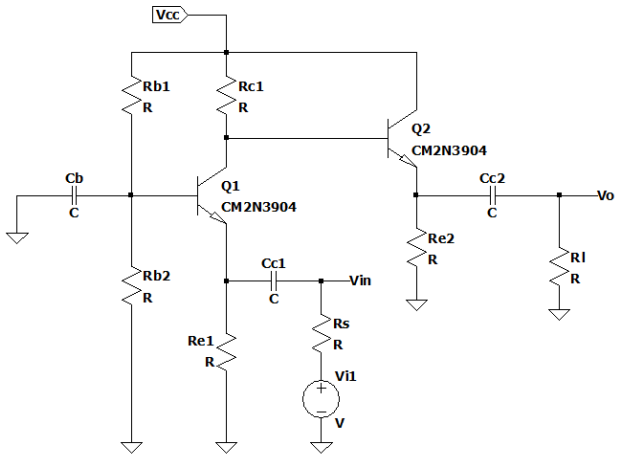

Figure 2-1 Cascaded common base/common collector Repeater

Part A – Biasing

In order to bias our amplifier, we first need to look at our circuits midband small signal equivalent model

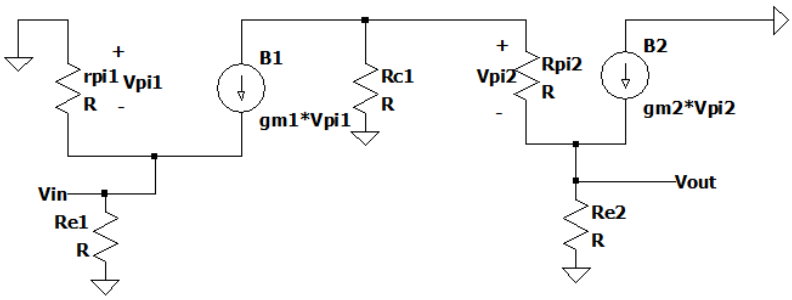

Figure 2-2 Midband equivalent circuit

From this model we can see that the input impedance

$$50\Omega = R_{in} = \left(\frac{r_\pi}{1+\beta}\right) \parallel R_{E1} =$$

$$\left(\frac{\beta}{1+\beta}\right) * \frac{V_T}{I_{C1}} \parallel \frac{V_{E1}}{I_{E1}} = \frac{V_T}{I_{E1}} \parallel \frac{V_{E1}}{I_{E1}} \approx \frac{V_T}{I_{E1}}$$

Assuming that V_{E1} is sufficiently larger than V_T

Knowing that $V_T = 25mV$ we can find $I_{E1} \approx 0.5mA$

And our output impedance $50\Omega = R_{out} = \frac{R_{C1}+r_{\pi 2}}{1+\beta} \parallel R_{E2} \approx \frac{R_{C1}+r_{\pi 2}}{1+\beta} = \left(\frac{R_{C1}}{1+\beta} + \frac{V_T * R_{E2}}{V_{E2}}\right)$

Knowing I_{E1}we can begin biasing our circuit using 1/3rd rule on the dc equivalent circuit.

Knowing that Vcc = 12V, $I_{E1} = 0.5mA$, and by using the $\beta = 130$ found in the previous part, 1/3rd rule gives us the following:

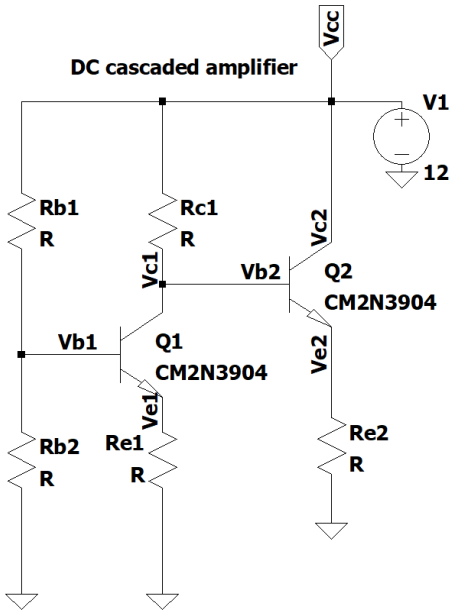

Figure 2-3 DC equivalent circuit

$$V_{E1} = 4V, V_{B1} = 4.7V, V_{C1} = V_{B2} = \frac{2}{3}Vcc = 8V,$$

$$V_{E2} = V_{B2} - 0.7 = 7.3V,$$

$$I_1 = 0.1I_{E1} = 0.05mA, I_{b1} = \frac{1}{1+\beta} * 0.5mA = 3.8\mu A$$

$$I_{C1} = \alpha I_{E1} = 0.496mA$$

$$\boldsymbol{R_{b1}} = \frac{12-4.7}{0.05mA} = 146k\Omega, \mathbf{R_{b2}} = \frac{4.7}{I_1 - I_{b1}} = 101.7k\Omega,$$

$$\boldsymbol{R_{E1}} = \frac{4}{I_{E1}} = 8k,\ I_{B2} = \frac{1}{\beta+1} * I_{E2} = \frac{1}{1+\beta}\frac{V_{E2}}{R_{E2}},$$

$$\boldsymbol{R_{C1}} = \frac{12-8}{I_{C1}+I_{B2}} = \frac{4}{0.496m+\frac{7.3}{131*R_{E2}}}, \left(\frac{R_{C1}}{131} + \frac{0.025*R_{E2}}{7.3}\right) = 50$$

Solving the system of equations, we find $\boldsymbol{R_{E2} = 431\Omega}$, $\boldsymbol{R_{C1} = 6356\Omega}$

Determining capacitor values is significantly easier, we know the input and output impedance of our design, so we know the resistance seen by both of our coupling capacitors during low frequency analysis, if we make C_B big enough that it shorts before C_{C1}. If we set $C_{C1} = C_{C2}$ and decide that they will be the dominant poles, then we can make the following approximation for the low frequency cut

$$1000Hz * 2\pi \geq\ \omega_{L3dB} = \sqrt{\left(\frac{1}{C_{C!} * 50}\right)^2 + \left(\frac{1}{C_{C2} * 50}\right)^2}$$

$$C_{C1} = C_{C2} \geq 4.501\mu F$$

Assuming C_B will short first we can set its value significantly higher to impose this. I chose C_B to be $22\mu F$ initially. Experimentally I found that C_B could be lowered to the $1\mu F$ level without causing the low cut to happen above 1000Hz

Part B – Standard values & impedance matching

Substituting in standard values for resistors and capacitors and then testing my circuits input and output impedance I found that they didn't meet specifications. R_{in} was 36Ω and R_{out} was 50Ω. In order to fix this low input impedance, I increased R_{E1} to $12k\Omega$ this increased my input impedance to 50Ω and increased the output impedance to 54Ω meeting the specifications.

Midband gain without load and source impedances was measured to be 40.183dB or 102V/V

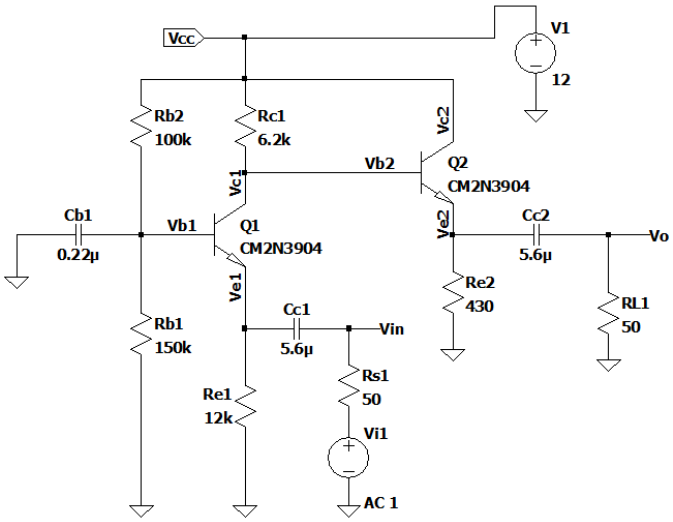

Figure 2-4: Finished circuit.

Part C – Bode plot & low-cut matching

Simulating the circuit and observing the bode plot and then lowering the value of C_B I found that you can lower C_B as low as $0.022\mu F$ at which point the low-cut point is just below 1000Hz. However, the condition is that C_B must be as low as possible without changing the low-cut point. I found this point to be at about $0.22\mu F$

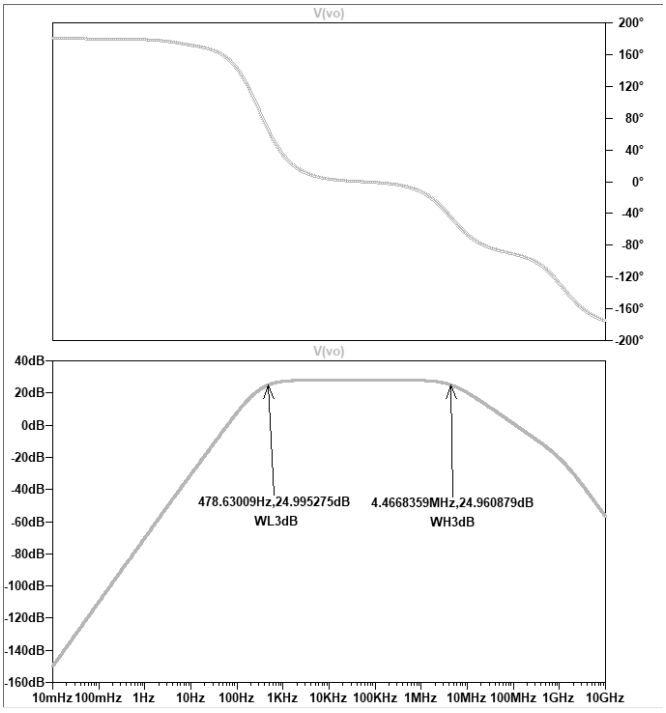

Figure 2-5: Bode plot of cascaded amplifiers Magnitude(bottom)& Phase (top)

Part 3 The Differential Amplifier:

Using the techniques, we learned in class we must design a differential amplifier, replacing the ideal current source with a current mirror for a more realistic realization of the design. We are given all the information needed to build the amplifier. In order to build the current mirror, we will need to make some observations. In order to decide the value of the reference resistor R_{ref} of the current mirror we need to determine the current I_{ref}. because we are building this current mirror out of 2 identical transistors we can use the equations we learned in class to find $I_{ref} = I_o * (1 + \frac{2}{\beta})$ where I_o would be the current of our ideal current source, in this case it is about 2mA since the currents leaving $I_{E1} = I_{E2} = 1mA$. Using $\beta = 300$ as it is the transistor model's maximum possible β and V_{BE} = 0.7V we see that $I_{ref} = 2.013mA \approx 2mA$ giving us a $R_{ref} = \frac{0-(-15+0.7)V}{2mA} = 7150\Omega$

We weren't given a load or source impedance, so I added an arbitrary load resistance of $10k\Omega$ and a source impedance of 50Ω in order to better match what we did in class. The load resistance of $10k\Omega$ is meant to be a general approximation of the input impedance of another differential amplifier.

Part A – Wiring and Bode plots

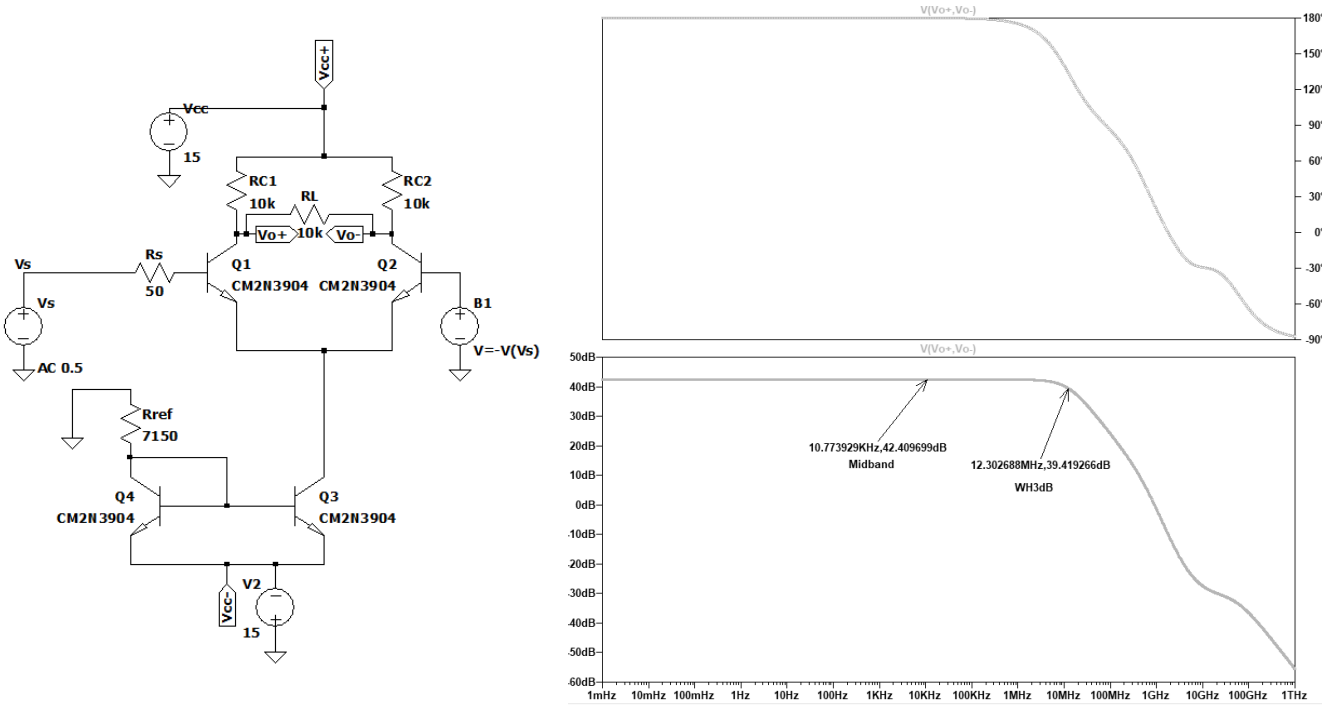

Figure 3-1: Bode plot of differential amplifier phase (top) and magnitude (bottom)

As shown by the bode plot our midband gain is approximately 42.4 dB = 132 V/V and our high frequency cut point is at about 12.3 MHz.

Part B – Comparison of calculations

In order to calculate the high frequency cut point and the differential gain I first took the dc operating point of my circuit in order to determine the β, gm, C_μ, C_π, and $r_\pi$values for the 2 identical transistors responsible for the differential amplifier. Using the small signal parameters given by LTspice after running a dc operating point analysis, I get $\beta = 120, gm = 0.041, r_\pi = 3500\Omega, C_\pi = 23.5\,pF, C_\mu = 1.9\,pF$

In order to calculate the high frequency poles of our differential amplifier we first build the high frequency model of our circuit.

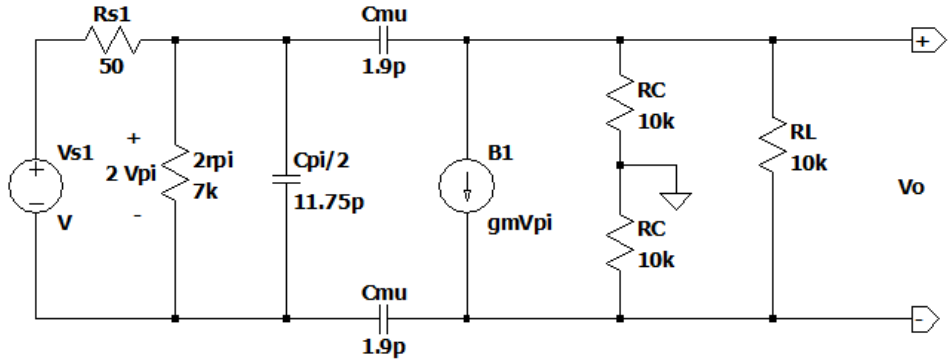

Figure 3-2: High frequency model

From this circuit we perform a miller transformation

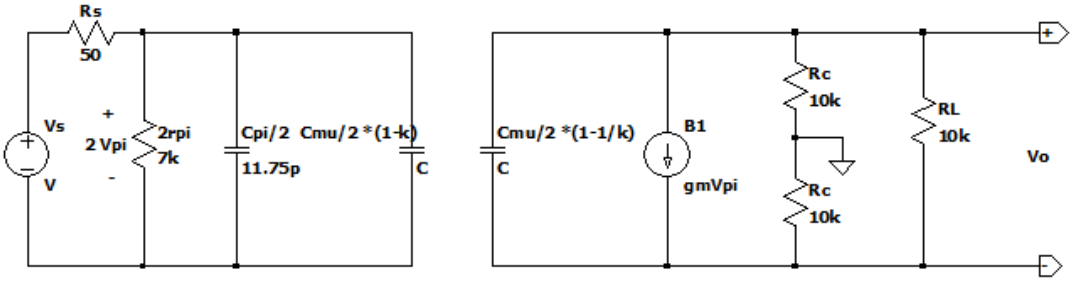

Figure 3-3: Miller equivalent model

From this miller transformation we can see that the equations of our high frequency poles are

$$\omega_{HP1} = \left(\left[\frac{C_\pi}{2} + \frac{C_\mu}{2} * (1-k)\right] * 2r_\pi \parallel R_s\right)^{-1} = 141.4M\frac{rad}{s} = 22.5MHz \; and$$

$$\omega_{HP2} = \left(\frac{C_\mu}{2} * \left(1 - \frac{1}{k}\right) * R_L \parallel 2R_C\right)^{-1} = 156.74M\frac{rad}{s} = 24.9MHz$$

Giving $(\omega_{H3dB})^{-1} = \sqrt{\left(\frac{1}{\omega_{Hp1}}\right)^2 + \left(\frac{1}{\omega_{Hp2}}\right)^2} \therefore \omega_{H3dB} = 105M\frac{rad}{s} = 16.7MHz$

Where $k = -gm * R_C * \frac{R_L}{R_L+2R_C} = -136.6$

Altering our high frequency model by opening all the capacitors we obtain the midband model and can see that the differential gain

$$A_M = -gm * R_C \left(\frac{2r_\pi}{2r_\pi+R_s}\right)\left(\frac{R_L}{R_L+2R_C}\right) = -135.7\ \frac{V}{V}$$

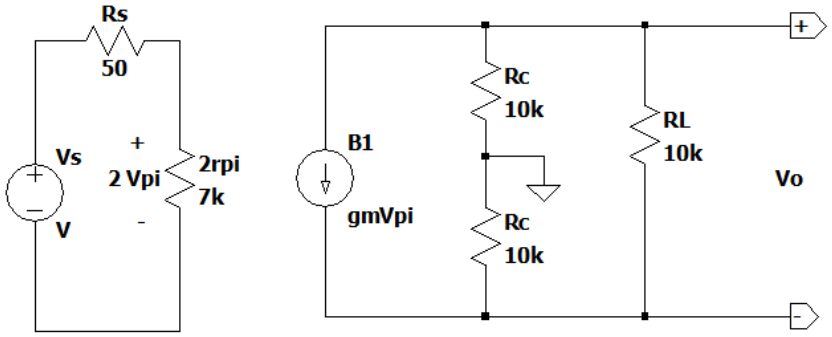

Figure 3-4: Midband equivalent circuit

When we compare our calculated values to the measured values obtained from our bode plot, we can see that our calculated values are very close to our measured and are an accurate approximation of our final circuit.

For the sake of completeness, I also found the mid band gain for no load to be about 370V/V with a high 3dB point at 4.5MHz measured and 407V/V and 36MHz calculated.

Part C – Differential output voltage

By setting my input voltage source to a midband frequency of 10kHz and then setting up my simulation to step through amplitude values from 0 to 250mV I plotted and observed the point where the output sinusoid begins to flatten and stops reflecting the original perfect sinusoid of the input source. I found the point where the output signal viewed in the time domain became nonlinear to be at an input voltage of approximately 25mV Peak = 50mV difference between the 2 sides of the differential amplifier.

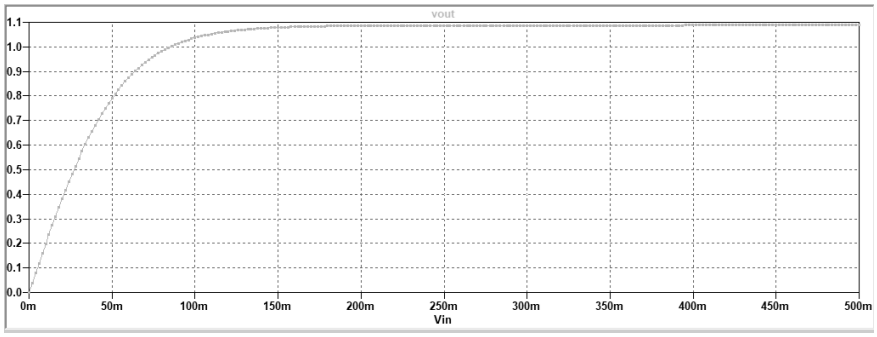

Figure 3-5:Vin vs Vout peak to peak

Part 4 The AM Modulator:

We were given an Am modulator circuit[1] and asked to apply several different source signals and observe the output signals. We were first asked to supply a 1kHz sine wave signal, then to observe what would happen with different signal amplitudes between 10mV and 100mV. We then repeated the process with a square wave instead of a sine wave.

Part A – Differential output observations

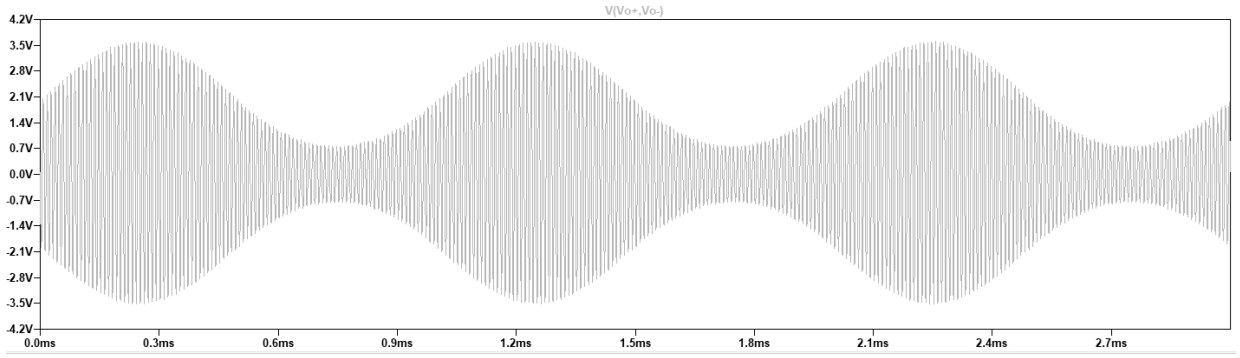

Figure 4-1: Amplitude modulation example of 1kHz carrier and 100kHz signal

As we can clearly see in figure 4.1, we have a signal which consists of a high frequency sinusoid whose amplitude is dependant on a second lower frequency sinusoid. This is a modulated wave where the smaller 1000Hz signal is carrying a larger 100kHz frequency signal.

Part B – Varying input amplitude

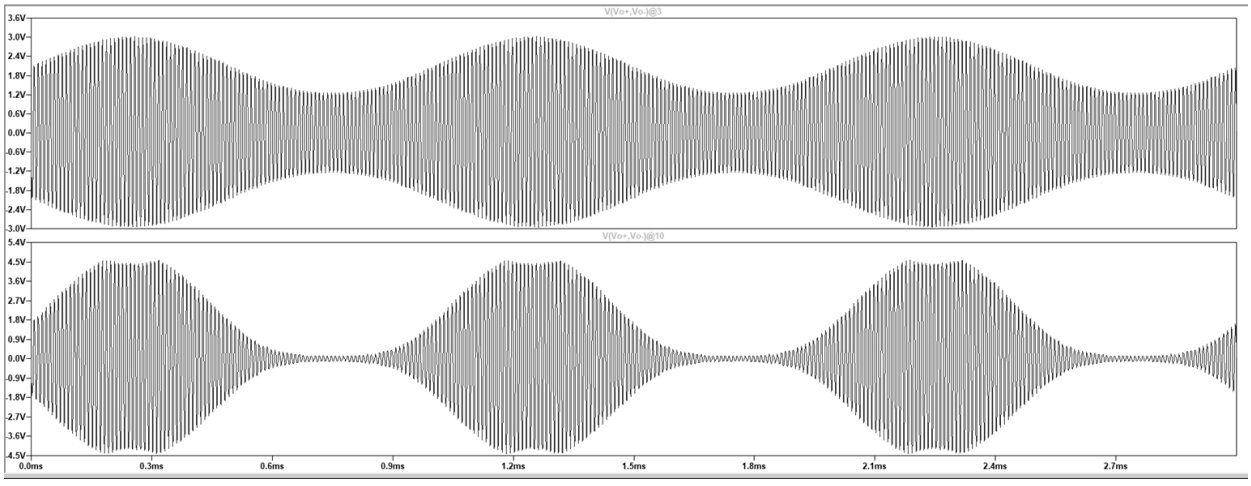

Figure 4-2: a comparison of 30mVpk signal(top) and 100mVpk signal(bottom)

As the input amplitude increases, we eventually begin to see clipping in our output as we would expect. Experimentally I found the amplitude where clipping begins to be at about

[1] Appendix figure 2

86mV. It can also be observed that the valleys of the modulated sinusoid get closer to 0 as the input amplitude increases. If we were to continue to increase the voltage, we would also see that the clipping of the signal begins to take the form of a sinusoid as shown in the appendix.

This signal being able to carry another signal is particularly interesting to me as, if I'm understanding it correctly, it means you can potentially send out a signal of information within a carrier frequency and have a receiver filter out signals of different frequencies in order to only capture the carrier frequency and then decompose the signal being carried into back information.

Part C – Square wave

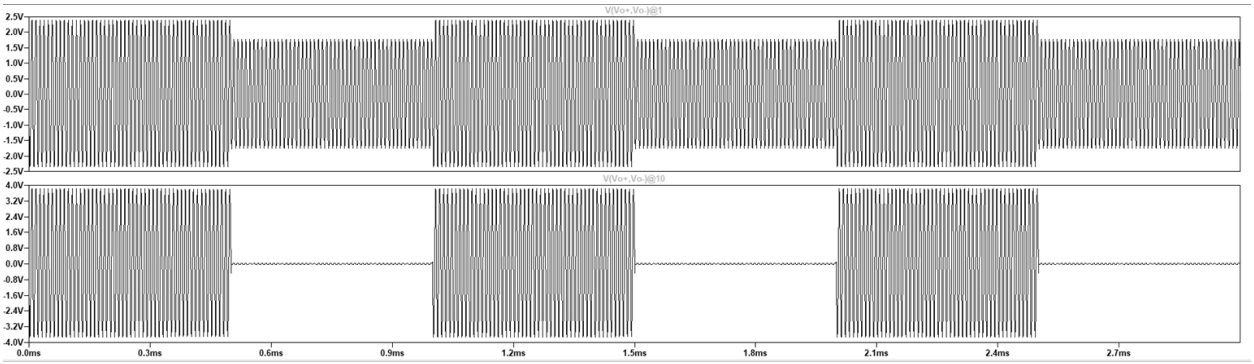

Figure 4-3: A comparison of 10mVpk signal(top) and 100mVpk signal(bottom) square wave input

As expected, the modulated wave became similar in shape to a square wave, mimicking the input signal that is now a square wave. This is desirable seeing how when the signal reaches saturation we don't see a dip at the peak, everything remains flat. Experimentally I found the point of saturation where the signal begins getting clipped to be about 86mV which is the same as for a sinusoidal signal.

Conclusion:

Throughout this project we simulated and tested 3 types of amplifier configurations using npn transistors.

We biased, designed, and simulated a cascode amplifier using the 1/4th rule. Then we calculated the expected cut frequencies and midband gain values and compared them to our simulated values. Comparing the 2 sets of values we validated our equations as an accurate approximation of the cascode amplifier. We then measured the input and output impedance and the saturation point of our cascode amplifier to prove that our design met specifications and operated as intended.

We designed a common base common collector repeater to have an input and output impedance of 50 Ω. Using the 1/3rd rule to bias the common base amplifier and then the common emitter we gained experience manipulating the equations and making educated assumptions to simplify the math and find a general approximation for the values of resistors

and capacitors to meet the requirements. We then simulated and adjusted our design in order to use less expensive components and better meet the specifications.

We used the techniques learned in class to design a differential amplifier with current mirror. We simulated and measured the midband gain as well as the high frequency cut point and compared them to our calculations. Our calculations managed to hold up to the simulation being able to stay within an order of magnitude of the measured values.

And finally, we built an AM modulator circuit and simulated it to see how different signals change when passed through an amplitude modulator. This felt more like an introduction to amplitude modulation and showed the potential of what can be done with differential amplifiers.

Overall I feel like I learned a fair bit about the design process, part 2 specifically showed that it can be much more efficient to simplify the numbers and find a general approximation that is easily fixed through simulation and that through simulation we can better meet our design specifications and reduce costs of a design.

Appendix:

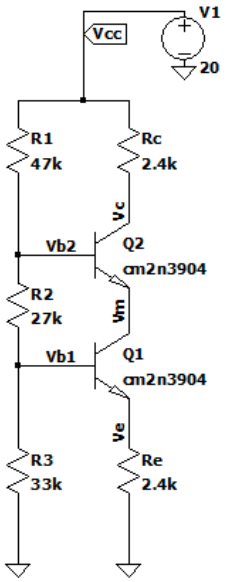

Figure A-0-1: DC equivalent biased cascode

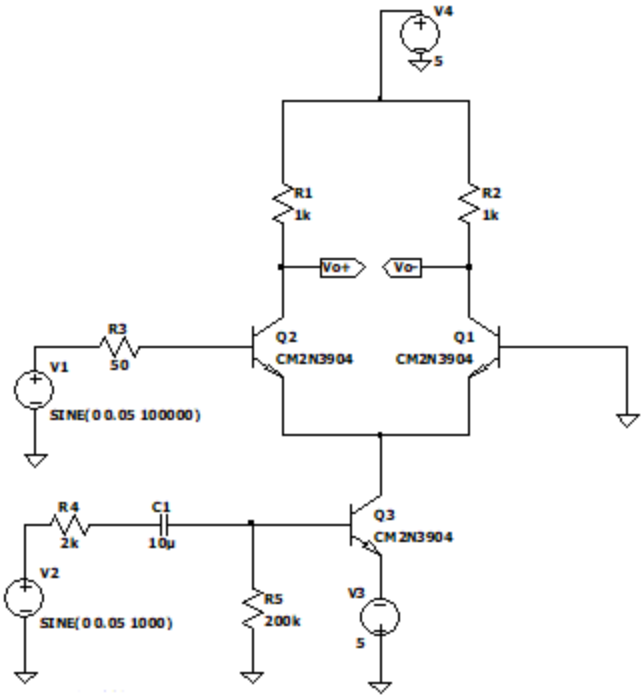

Figure A-0-2: provided AM modulator circuit

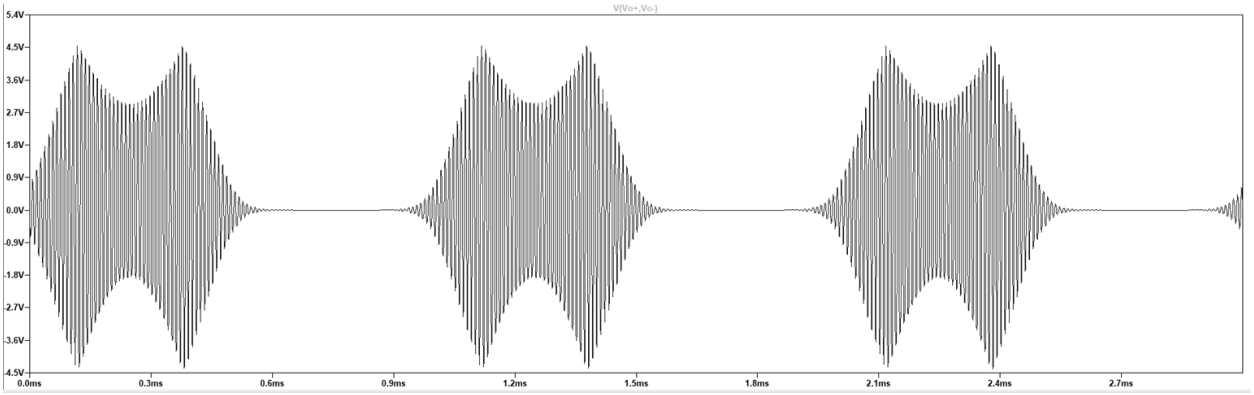

Figure A-0-3: 200mVpk sine wave signal for part 4c